CMOS SIGE CHANNEL PFET AND SI CHANNEL NFET DEVICES WITH MINIMAL STI RECESS

BACKGROUND OF THE INVENTION

The present invention relates generally to a semiconductor device and method of forming the same and, more specifically, to CMOS SiGe channel pFET and Si channel nFET devices.

For certain technology node device requirements, it may be necessary to use different channel materials on nFET and pFET devices. The channel materials may be grown using epitaxial growth techniques. In high-k/metal-gate technologies, silicon germanium (SiGe) may be used as the pFET channel material to assist in reaching a desired pFET metal-semiconductor workfunction, while maintaining a traditional silicon channel for the nFET devices. When using epitaxial growth for channel materials on a desired device, a hardmask material such as silicon dioxide (SiO2) or silicon nitride (SiN2) may be used to protect against growth of new channel material on the other devices. The hardmask material is then removed.

Nitride hardmasks are usually not used when growing silicon germanium (SiGe) channel materials. The etchant, such as hot phosphoric acid, used to remove the nitride hardmask also etches the silicon germanium (SiGe) material itself. Patterning of oxide hardmasks with common oxide etchants, such as hydrofluoric acid, also etches the shallow trench isolation (STI) oxide resulting in a different step-height (STI oxide height relative to channel silicon) between nFET and pFET devices. Different size STI divots (amount of STI oxide pulldown immediately next to the active silicon device) may also occur between nFET and pFET devices. Step-height differences and divot differences can create structural topography problems in downstream processing as well as electrical device issues, such as leakage, performance, active width and corner device. A large difference can exist between STI areas and active silicon areas in pFETs versus nFETs. This is all driven by the patterning of the hardmask layer used to protect the nFET device from receiving epitaxial growth. The size of the STI divots near the edge of the active silicon are drastically asymmetrical.

SUMMARY OF THE INVENTION

In a first aspect of the invention, a method of forming a device includes providing a wafer having a pad oxide layer, the wafer including a silicon substrate having nFET regions and pFET regions. The method includes removing the pad oxide layer to expose a silicon channel above the nFET regions and the pFET regions. The method includes growing an epitaxial layer on the silicon channel. The method includes applying a positive photoresist layer on the epitaxial layer above the pFET regions. The method further includes removing the epitaxial layer above the nFET regions. The method also includes removing the positive photoresist layer.

In a further aspect of the invention, a method of forming a device includes the following steps in the order named. The method includes providing a wafer having a pad oxide layer, the wafer including a silicon substrate and having nFET regions and pFET regions. The method includes removing the pad oxide layer to expose a silicon channel above the nFET regions and the pFET regions. The method includes performing a wet oxide etch preclean on the silicon channel. The method includes growing a silicon germanium (SiGe) epitaxial layer on the silicon channel, wherein the silicon germanium (SiGe) epitaxial layer is directly connected to the silicon channel and functions as part of the silicon channel. The method includes depositing a hardmask layer on the silicon germanium (SiGe) epitaxial layer. The method includes applying a positive photoresist layer on the hardmask layer above the pFET regions. The method includes removing the hardmask layer above the nFET regions. The method includes removing the positive photoresist layer. The method further includes removing the silicon germanium (SiGe) epitaxial layer above the nFET regions. The method also includes removing the hardmask layer above the pFET regions.

In a further aspect of the invention, a method of forming a device includes the following steps in the order named. The method includes providing a wafer having a pad oxide layer, the wafer including a silicon substrate and having nFET regions and pFET regions. The method includes removing the pad oxide layer to expose a silicon channel above the nFET regions and the pFET regions. The method includes performing a wet oxide etch preclean on the silicon channel. The method includes growing a silicon germanium (SiGe) epitaxial layer on the silicon channel, wherein the silicon germanium (SiGe) epitaxial layer is directly connected to the silicon channel and functions as part of the silicon channel. The method includes depositing a first hardmask layer on the silicon germanium (SiGe) epitaxial layer. The method includes depositing a second hardmask layer on the first hardmask layer. The method includes applying a positive photoresist layer on the second hardmask layer above the pFET regions. The method includes removing the second hardmask layer above the nFET regions. The method includes removing the positive photoresist layer. The method includes removing the first hardmask layer above the nFET regions. The method includes removing the silicon germanium (SiGe) epitaxial layer above the nFET regions. The method further includes removing the second hardmask layer above the pFET regions. The method also includes removing the first hardmask layer above the pFET regions.

In a yet further aspect of the invention, a device includes a wafer, the wafer having a silicon substrate having nFET regions and pFET regions. The device further includes a silicon channel above the nFET regions. The device also includes an epitaxial layer above the pFET regions.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention is described in the detailed description below, in reference to the accompanying drawings that depict non-limiting examples of exemplary embodiments of the present invention.

FIGS. **1**A-**1**K show a starting structure, processing steps and a final structure in accordance with a first embodiment of the invention;

FIGS. **2**A-**2**I show a starting structure, processing steps and a final structure in accordance with a second embodiment of the invention;

FIGS. **3**A-**3**K show a starting structure, processing steps and a final structure in accordance with a third embodiment of the invention;

FIGS. **4**A-**4**F show a starting structure, processing steps and a final structure in accordance with a fourth embodiment of the invention; and

FIGS. **5**A-**5**I show a starting structure, processing steps and a final structure in accordance with a fifth embodiment of the invention.